## ABSTRACT OF THE DISCLOSURE

A method and apparatus for evaluating the design quality of an integrated circuit design. The design to be evaluated comprises a plurality of static gates, such as, for example, NAND and NOR gates. The apparatus of the present invention comprises a computer configured to execute a rules checker program. The rules checker program analyzes each of the static gates to determine whether or not the gates meet acceptable noise immunity requirements. In order to perform this task, the rules checker program constructs models of each gate. The models emphasize or de-emphasize the strengths of certain FETs of the gate in response to noise on inputs to the gate for different logic states of the inputs. For each model, the rules checker program obtains a PFET-to-NFET width ratio. These ratios are utilized to obtain noise levels from a lookup table. Noise levels on the inputs to the gate are derived, either by calculation or simulation. These derived noise levels are then compared with the noise levels obtained from the lookup table to determine whether or not the gate being evaluated meets acceptable noise immunity requirements.